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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,692	12/04/2003	Jingkuang Chen	D/A1591D	8664

7590 04/11/2005

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EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,692	CHEN ET AL.	
	Examiner	Art Unit	
	Nema O. Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-14 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-14 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02092005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment, filed 1-25-05 which has been entered and considered. Cancellation of claims 2 and 15-16 is acknowledged; claims 1, 3-14, and 17-21 remain pending.

Claim Rejections - 35 USC § 112

The rejection of claims 9-11 under 35 USC 112 second paragraph, made in prior Office Action is hereby withdrawn, subsequent to corrections made by Applicant in paper filed 1-25-05.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 13, 17, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Waters et al. (6,546,798). Waters discloses a heterogeneous device, comprising: a substrate (Fig.5A no #); and a plurality of heterogeneous circuit devices defined in the substrate; and a photodiode defined in the substrate (col.3 lines 56-67) **[claim 13]**. Waters also discloses wherein the substrate comprises a layer of silicon (col.3 lines 63-

67) **[claim 17]**; and at least one microelectromechanical system-based element defined in the substrate (col.1 lines 14-20; col.3 lines 63-65) **[claim 21]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5, 8-12, 14, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waters as applied to claim 13 above, and further in view of Smayling et al. (5,242,841). Waters is silent concerning a high or low voltage well, or p-type silicon, or a field oxide layer, or contacts to sources/drains, or a double diffused MOS device. However, Waters would look to one such as Smayling to form a lateral diffused MOS device because Smayling discloses a high voltage well (Fig.2h el.182) of a first circuit device (el.142) defined in the substrate; a first low voltage well (el.190) of a second circuit device (el.140) defined in the substrate; and a second low voltage well (el.175) of the second circuit device defined in the substrate. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the wells of Smayling with the device of Waters in order to form a lateral diffused MOS device (col.10 lines 3-15) **[claims 1, 8]**. Based upon the rejection of claim 1 above, Waters also discloses further comprising at least one microelectromechanical system-based element defined in the substrate (col.1 lines 14-20; col.3 lines 63-65) **[claim 3]**;

wherein the substrate comprises a layer of silicon (col.3 lines 63-67) **[claim 4]**; and further comprising a polysilicon gate (col.5 lines 36-40) **[claim 10]**.

Waters would look to one such as Smayling to form a CMOS device because Smayling discloses wherein the layer of silicon comprises p-type silicon (col.4 lines 38-43). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the p-type silicon of Smayling with the device of Waters in order to form a CMOS device, as Waters discloses (Waters – col.5 lines 57-63) **[claims 5, 18]**.

Waters would look to one such as Smayling for device isolation because Smayling discloses a field oxide layer (el.210) over at least part of each of the high voltage well, the first low voltage well and the second low voltage well. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the field oxide layer of Smayling with the device of Waters in order to provide device isolation **[claim 9]**.

Waters would look to one such as Smayling for surface contact regions because Smayling discloses a P-body (Fig.2k el.182) defined in the high voltage well of the first circuit device (el.142); an N+ source/drain defined in each of the P-body, the high voltage well and the first low voltage well of the second circuit device; and a P+ source/drain in each of the P-body and the second low voltage well of the second circuit device (col.6 lines 51-65). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the field oxide layer of

Smayling with the device of Waters in order to form surface contact regions (col.6 lines 60-65) **[claim 11]**.

Waters would look to one such as Smayling for interconnection because Smayling discloses a passivation oxide layer over at least the field oxide layer (col.6 lines 8-15) and the polysilicon gates (col.6 lines 38-50); a plurality of vias through the passivation oxide layer; and a plurality of contacts, each of the contacts extending through the vias and contacting at least one of the sources/drains (col.6 line 66 – col.7 line 15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the oxide layer, vias, and contacts of Smayling with the device of Waters in order to form metal interconnects (col.7 lines 11-13) **[claim 12]**.

Based upon the rejection of claim 13 above, Waters discloses wherein the plurality of heterogeneous circuit devices comprises at least one complementary metal oxide semiconductor transistor col.5 lines 57-63). However, Waters does not disclose a double diffused MOS device. Waters would look to one such as Smayling for implementation of high power devices because Smayling discloses at least one double-diffused metal oxide semiconductor transistor (col.2 lines 36-46). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the double diffused MOS device of Smayling with the device of Waters in order to implement high power devices on a single substrate (col.1 lines 22-27) **[claim 14]**.

Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waters as applied to claim 13 above, and further in view of Kubena et al. (6,580,138).

Waters does not disclose a silicon-on-insulator (SOI) wafer. However, Waters would look to one such as Kubena for structural stability because Kubena discloses wherein the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween (col.4 line 66 – col.5 line 8; col.5 lines 17-19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the SOI device of Kubena with the device of Waters in order to provide a single crystal structure with better structural stability (Kubena – col.1 lines 47-63). Kubena also discloses wherein the single-crystal-silicon layer comprises p-type silicon (col.5 lines 50-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the p-type silicon of Kubena with the device of Waters in order to provide a CMOS device, as Waters discloses (Waters – col.5 lines 57-63).

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waters in view of Smayling as applied to claims 1 and 13 above, and further in view of Kubena et al. (6,580,138). Waters and Smayling do not disclose a silicon-on-insulator (SOI) wafer. However, Waters and Smayling would look to one such as Kubena for structural stability because Kubena discloses wherein the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween (col.4 line 66 – col.5 line 8; col.5 lines 17-19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the SOI device of Kubena with the device of Waters and Smayling in order to

provide a single crystal structure with better structural stability (Kubena – col.1 lines 47-63). Kubena also discloses wherein the single-crystal-silicon layer comprises p-type silicon (col.5 lines 50-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the p-type silicon of Kubena with the device of Waters and Smayling in order to provide a CMOS device, as Waters discloses (Waters – col.5 lines 57-63).

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O. Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

CRAIG A. THOMPSON
PRIMARY EXAMINER